A Detailed Comparison of TPC-C versus TPC-B

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Online Transaction Processing (OLTP)

- Major workload for high performance servers
- OLTP characterization
  - Large number of clients
  - Short transactions that update small amounts of data

- Transaction Processing Council OLTP benchmarks
  - TPC-B: Models a large bank with multiple branches
  - TPC-C: Models a warehouse distribution center

- How does processor and memory system performance of TPC-B and TPC-C compare?
TPC-B versus TPC-C

- Evaluated scaled-down models of these two benchmarks
  - performance monitoring of cutting-edge hardware
  - full-machine simulation of next generation hardware

- Similarities
  - both show similar speedups from out-of-order execution
  - working sets of both can fit in reasonably sized on-chip L2

- Difference
  - TPC-B suffers from high sharing overheads

- Overall, both benchmarks have very similar processor and memory system characteristics!
TPC-C vs. TPC-B

- Introduction
- Workload scaling
- Performance monitoring
- Simulation
- Conclusion
Workloads

• TPC-B Model
  – 40 branches
  – Size: 1.2GB disk, 900MB in-memory
  – 8 server processes per processor

• TPC-C Model
  – 8 warehouses
  – Size: 3.0GB disk, 800MB in-memory
  – 8 server processes per processor

• Both built on Oracle
Performance Monitoring: Platform

• Monitoring via IProbe and Continuous Profile Infrastructure

• Eight processor AlphaServer (AS) 8400
  – Alpha 21164 processor at 612MHz
    • three cache levels: 8K/1-way, 96K/3-way, 4MB/1-way
    • memory latency: board-level cache hit 55 ns, memory 360 ns, dirty miss 542 ns

• Two processor AS DS20
  – Alpha 21264 processor at 500MHz
    • two cache levels: 64K/2-way, 4MB/1-way
    • memory latency: L2 hit 38ns, memory 190 ns, dirty miss 350 ns
Monitoring: AS 8400

8 processors

<table>
<thead>
<tr>
<th></th>
<th>TPC-B</th>
<th>TPC-C</th>
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<tbody>
<tr>
<td>icache miss rate</td>
<td>12.4%</td>
<td>13.3%</td>
</tr>
<tr>
<td>dcache miss rate</td>
<td>31.7%</td>
<td>31.5%</td>
</tr>
<tr>
<td>scache miss rate</td>
<td>7.4%</td>
<td>7.1%</td>
</tr>
<tr>
<td>bcache miss rate</td>
<td>1.6%</td>
<td>1.0%</td>
</tr>
<tr>
<td>CPI</td>
<td>11.8</td>
<td>5.9</td>
</tr>
<tr>
<td>% dirty misses</td>
<td>26.8%</td>
<td>9.4%</td>
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Monitoring: AS DS20 vs. AS 8400

- Both machines use 2 processors
- Differences
  - DS20 has 21264 processor with out-of-order execution
  - DS20 has faster memory subsystem

- TPC-B
  - Speedup is 2.44x on AS DS20

- TPC-C
  - Speedup is 2.42x on AS DS20
Simulation: SimOS-Alpha Environment

- Full system simulation including kernel activity
  - kernel component approximately 20% of execution time
- Multiple levels of detail
  - single-issue in-order processor
  - quad-issue out-of-order processor
Simulation: Platform

- Eight processor “next-generation” AlphaServer
  - Alpha processor (1GHz)
    - single-issue, in-order and four-issue, out-of-order pipelines
    - integrated on-chip L1, L2, memory, coherence, and network controllers
      - L1: various sizes, 2-way associative
      - L2: various sizes and associativities
  - NUMA architecture
    - L2 Hit: 15 ns
    - local memory latency: 75 ns
    - remote memory latency: clean 150 ns, dirty 200 ns
Simulation: In-order vs. Out-of-order

- Out-of-order execution speedup
  - TPC-B: 1.32x
  - TPC-C: 1.38x
Simulation: Impact of L1 Cache Size

- Execution time speedup of 128K L1 relative to 32K L1
  - TPC-B: 1.12x
  - TPC-C: 1.09x
Simulation: Impact of L2 Configuration

- TPC-B shows similar trends [Barroso, et al 1998]
Conclusions: TPC-B vs. TPC-C

• Both benchmarks spend majority of time in the memory system
  – out-of-order execution is not effective in hiding memory stalls
  – working sets fit in reasonably sized associative on-chip L2

• TPC-B has higher sharing and memory system overhead
  – more dirty misses
  – higher L1 miss rate

• *Benchmarks are very similar in processor and memory system characterizations!*